

**ABSTRACT**

A cache memory related to the present invention is a cache memory employing a set associative system, for  
5 generating a valid bit for showing the presence of  
validity of a cache data, and comprises a tag memory 1 for  
storing an address tag of an address of a cache data and a  
first valid bit for showing the presence of validity of  
the cache data in a set of blocks in response to an index,  
10 and a valid bit register 2 for storing a second valid bit  
corresponding to the first valid bit, and resetting the  
second valid bit, and the valid bit is generated based on  
the first valid bit and the second valid bit.